University of California, Santa Barbara
Department of Electrical and Computer Engineering

ECE 152A – Digital Design Principles

Midterm Exam #1 – Solution
July 15, 2009

Name _____

Perm # _____

Lab Section   _____

Problem #1 (20 points) _____

Problem #2 (20 points) _____

Problem #3 (20 points) _____

Problem #4 (20 points) _____
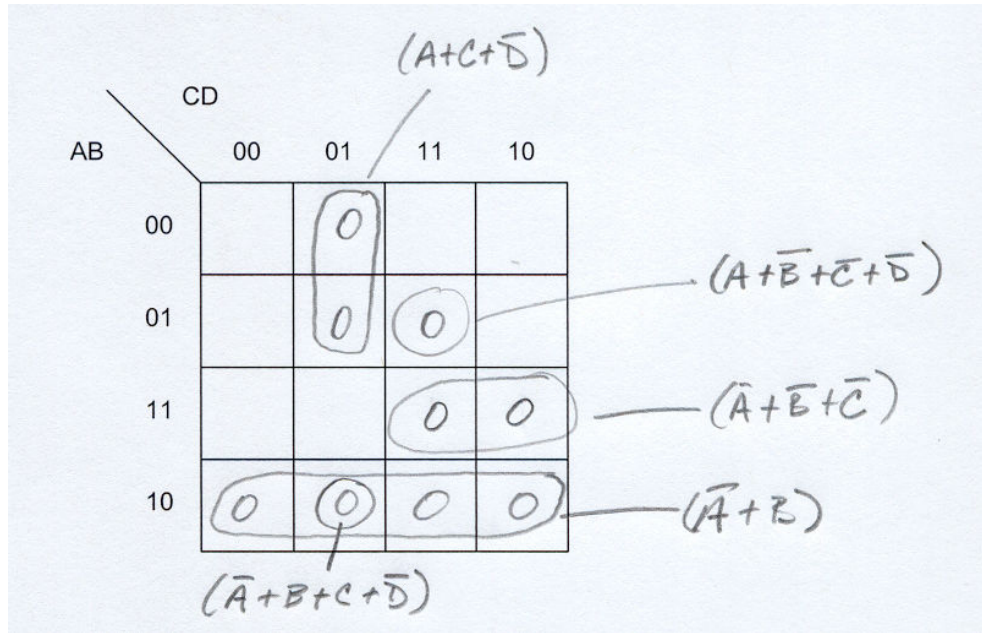
Problem #5 (20 points) _____

Total   (100 points) _____

- This is a 75 minute exam; closed book, closed notes, no calculators.
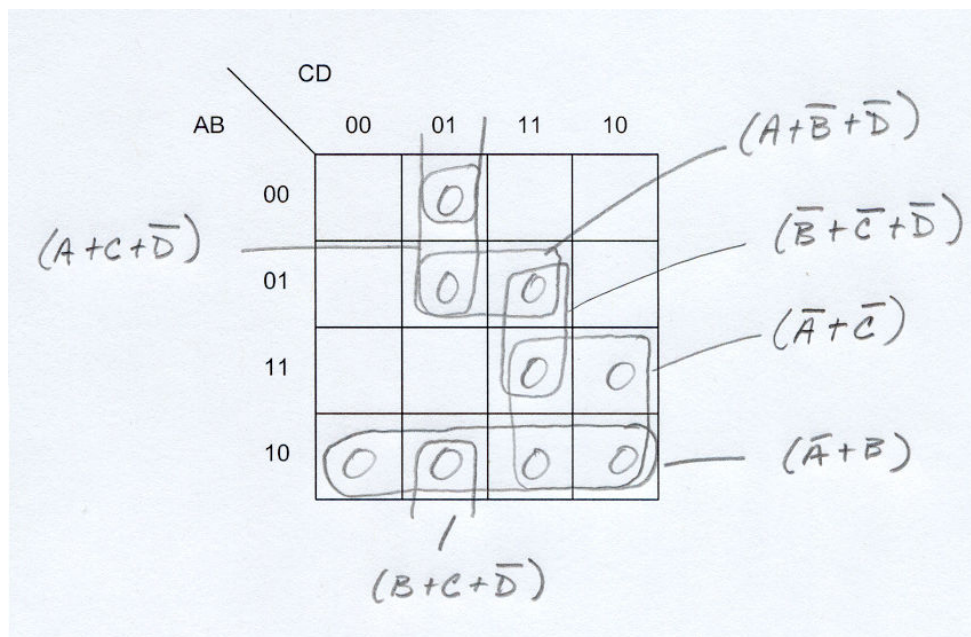- Answer all questions on the exam.

Problem #1.

a) Map and identify the sum terms for the following function on the Karnaugh map.

$$f = (A+C+D')(A+B'+C'+D')(A'+B'+C')(A'+B)(A'+B+C+D')$$

b) Copy the Maxterms from the above map and identify all the prime implicants for a product of sums implementation.

c) List the essential prime implicants for the product of sums implementation.

$$(\bar{A}+\bar{C})$$

$$(\bar{A}+B)$$

d) Construct a minimal product of sums implementation of this function. Is this expression unique (and why or why not)?

$$(\bar{A}+\bar{C})(\bar{A}+B) \begin{cases} (\bar{B}+\bar{C}+\bar{D})(A+C+\bar{D}) \\ (A+\bar{B}+\bar{D})(B+C+\bar{D}) \\ (A+\bar{B}+\bar{D})(A+C+\bar{D}) \end{cases}$$

NOT UNIQUE

(NOT ALL
ESSENTIAL
PRIME IMPLICANTS)

e) For the same function, map the minterms on the Karnaugh map below, identify all the prime implicants and essential prime implicants and construct a minimal sum of products expression. Is this expression unique (and why or why not)?


$$= \bar{A}\bar{D} + AB\bar{C} + \bar{A}\bar{B}C$$

UNIQUE

ALL ESSENTIAL
PRIME IMPLICANTS
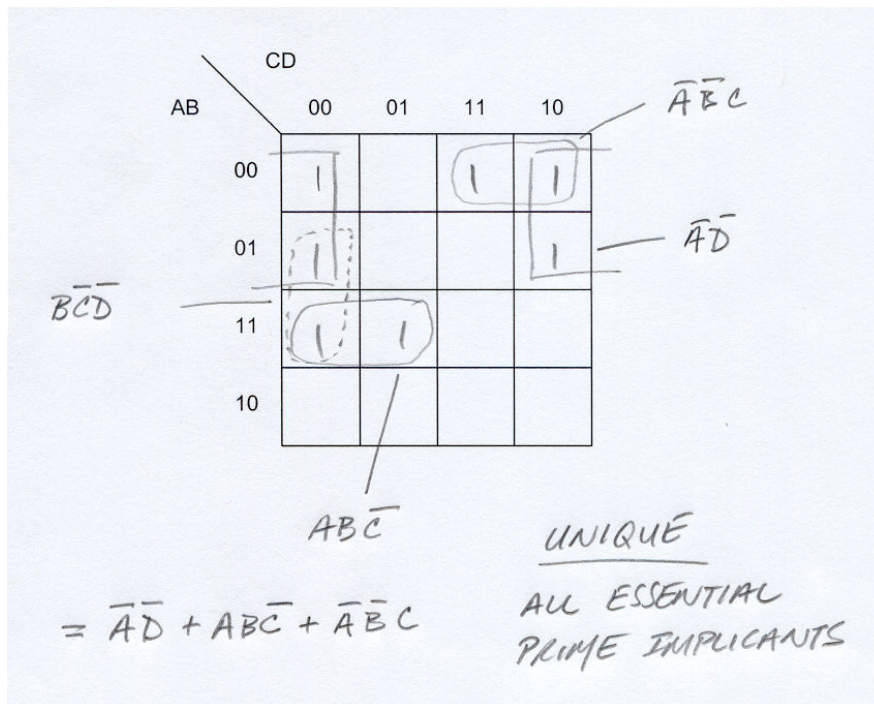
f) Using only Boolean algebra, convert the minimized product of sums expression in part d) to a sum of products representation. Note that the resulting product terms should be the same as the implicants on the Karnaugh map of part e) above.

$$(\bar{A}+\bar{B})(\bar{A}+\bar{C})(A+\bar{B}+\bar{D})(A+C+\bar{D})$$

$$(\bar{A}+\bar{B})$$

$$(\bar{A}+\bar{C})$$

$$\overline{\bar{A}\bar{A} + \bar{A}\bar{B} + \bar{A}\bar{C} + \bar{B}\bar{C}}$$

$$\bar{A} + \bar{B}\bar{C}$$

$$A + \bar{B} + \bar{D}$$

$$\overline{A\bar{A} + A\bar{B}\bar{C} + \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{A}\bar{D} + \bar{B}\bar{C}\bar{D}}$$

$$A\bar{B}\bar{C} + \bar{A}\bar{B} + \bar{A}\bar{D} + \bar{B}\bar{C}\bar{D}$$

$$A + C + \bar{D}$$

$$\overline{AA\bar{B}\bar{C} + A\bar{A}\bar{B} + A\bar{A}\bar{D} + A\bar{B}\bar{C}\bar{D}}$$

$$+ A\bar{B}\bar{C}C + \bar{A}\bar{B}C + \bar{A}C\bar{D} + \bar{B}\bar{C}\bar{D}C$$

$$+ A\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{D} + \bar{A}\bar{D}\bar{D} + \bar{B}\bar{C}\bar{D}\bar{D}$$

$$= A\bar{B}\bar{C} + A\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C + \bar{A}C\bar{D}$$

$$+ A\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{D} + \bar{A}\bar{D} + \bar{B}\bar{C}\bar{D}$$

$$= A\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}\bar{D} + \bar{B}\bar{C}\bar{D}$$

$$\underbrace{\qquad\qquad\qquad\qquad}_{\text{CONSENSUS TERM}}$$

$$= A\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}\bar{D}$$

Problem #2.

a) The figure below illustrates the voltage transfer characteristic (Vout vs. Vin) for a standard TTL circuit. On the figure, identify VOH, VIH, VOL and VIL.
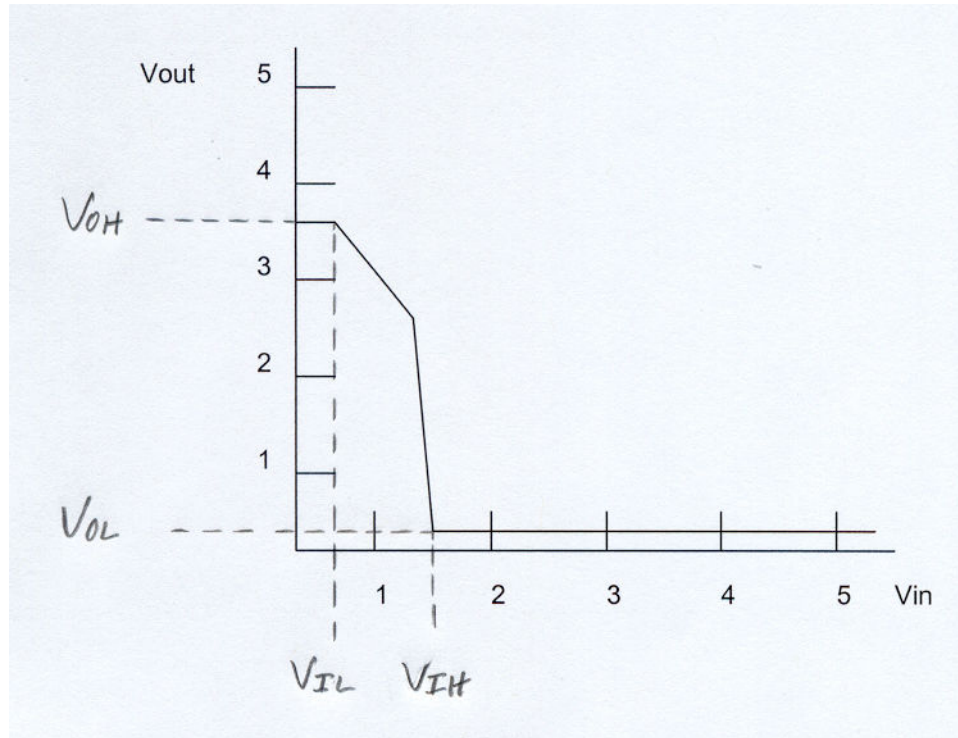

b) What are the approximate numeric values of VOH, VIH, VOL and VIL?

$$V_{OH} = 3.5V \qquad V_{OL} = 0.2V$$
$$V_{IH} = 1.5V \qquad V_{IL} = 0.5V$$

c) What are the values of the high and low noise margins?

$$NM_H = V_{OH} - V_{IH} = 2.0V$$
$$NM_L = V_{IL} - V_{OL} = 0.3V$$

Recall that in a static CMOS gate, pMOS transistors are used in the pull up network because they "pass a good 1" and nMOS transistors are used in the pull down network because they "pass a good 0". If we connect a pMOS transistor in parallel with an nMOS transistor as shown below, we construct a circuit known as a transmission gate which can pass both a good 0 and a good 1 (when both transistors are "on").
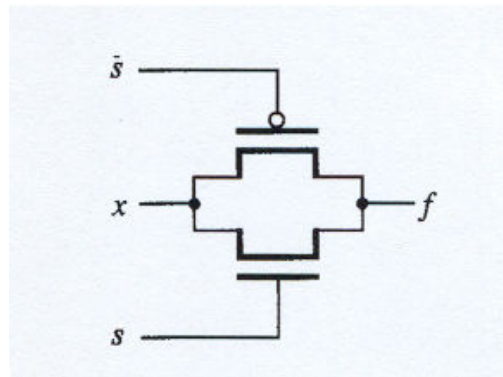

Note that the gates of the transistors are driven by complementary signals S (nMOS) and S' (pMOS).

We'll study digital design using transmission gates in detail later in the quarter, but you should understand the operation of the transmission gate based on your knowledge of static CMOS gates (inverter, NAND and NOR).

The symbol for the transmission gate is shown below.
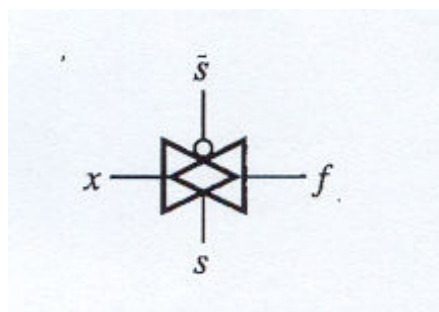
Construct the truth table for the circuit below consisting of two transmission gates and a single inverter. The inputs are x_1, x_2 and S; the output is f.
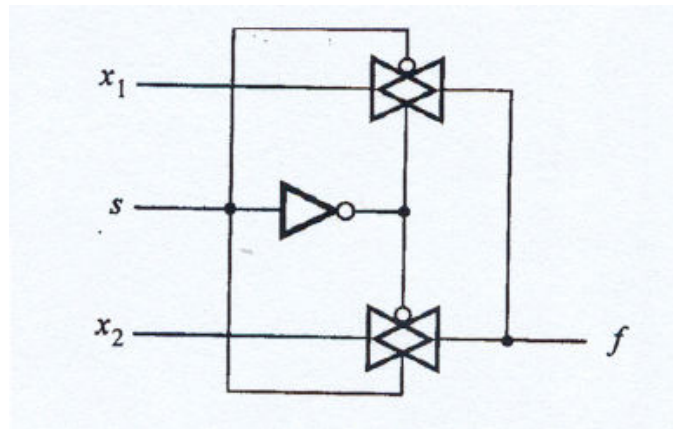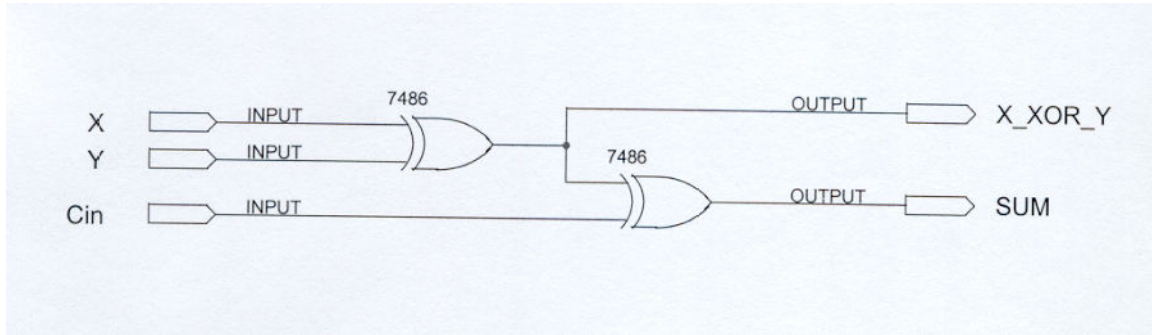

S	X_1	X_2	f	
0	0	0	0	
0	0	1	0	X_1
0	1	0	1	
0	1	1	1	
1	0	0	0	
1	0	1	1	X_2
1	1	0	0	
1	1	1	1	

Problem #3.

The schematic below illustrates the implementation of the SUM output of a full adder using 7486 TTL Exclusive OR gates and includes a pin out of the internal node X XOR Y.

The partial data sheet below includes the logical function, truth table, pin out and switching characteristics for the 7486. Note that the high to low and low to high propagation delays are dependant on the logical value of the "other" input.

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

86 $Y = A \oplus B = \overline{A}B + A\overline{B}$

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

See page 7-65

SN5486 (J, W)   SN7486 (J, N)
SN54LS86 (J, W)   SN74LS86 (J, N)
SN54S86 (J, W)   SN74S86 (J, N)

SN54L86 (J)   SN74L86 (J, N)

SN54L86 (T)

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	$C_L = 15$ pF, $R_L = 400$ Ω, See Note 3		15	23	ns
t_{PHL}					11	17	
t_{PLH}	A or B	Other input high			18	30	ns
t_{PHL}					13	22	

Complete the timing diagram for the X XOR Y and SUM outputs on the following page. Indicate all propagation delays on the timing diagram and identify the critical path and the input conditions that result in the maximum delay.
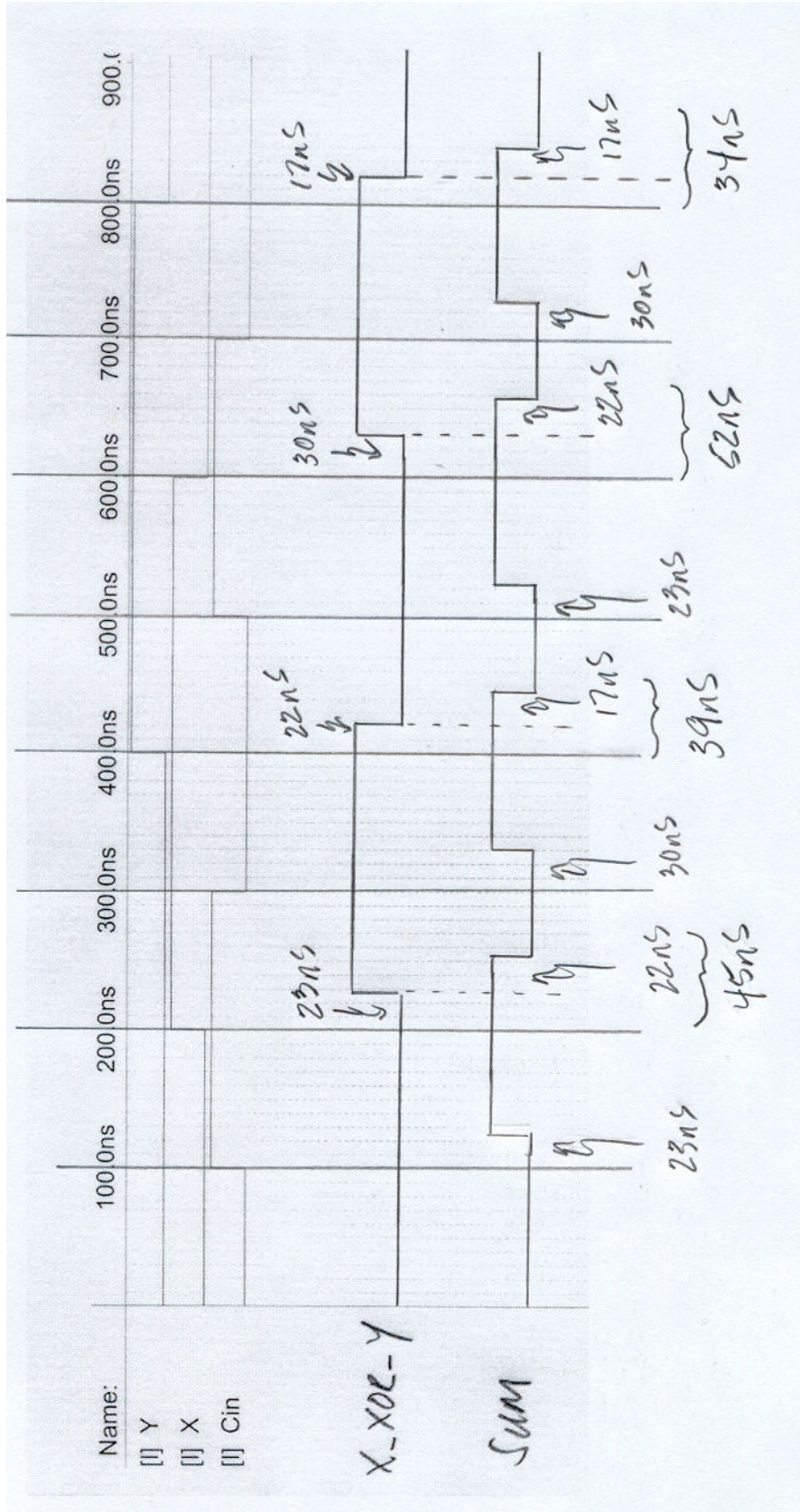
Problem #4.

In this problem, you are asked to design a portion of the circuitry in the COX$^{®}$ cable box/television remote control unit. The remote control has only 4 buttons labeled:

Power (P): toggles the power (on/off) to the television and/or the cable box. When the Power button is pressed, the Up/Down and Channel buttons are disabled.

TV (T): when pressed simultaneously with other buttons, controls the power and input to the television

Up/Down (U): controls the cable channel tuning when pressed alone or television input or cable channel tuning when pressed simultaneously with other buttons (see operation below).

Channel (C): controls the cable channel tuning when pressed alone or television input or cable channel tuning when pressed simultaneously with other buttons (see operation below).

The circuit has 5 outputs:

Cable Channel Up (CU): cable box channel is tuned up

Cable Channel Down (CD): cable box channel is tuned down

TV Input Select (TS): input to television is cycled (i.e., from antenna to component video to HDMI, etc.)

TV Power (TP): turns TV on or off

Cable Box Power (CP): turns cable box on or off

In general, the remote control unit operates the television when the TV (T) button is pressed and the cable box when it is not.

The unit should function as follows:

When the power button is pressed, both the television and cable box power signals become active (logic 1). If the power (P) and television (T) buttons are pressed simultaneously, only the television power signal becomes active.

When the channel button (C) or the up/down button (U) is pressed, the cable box is tuned to the next higher channel. When the channel button (C) is pressed simultaneously with the Up/Down button (U), the cable box is tuned to the next

lower channel. When the channel button (C) or the up/down button (U) is pressed simultaneously with the TV (T) button, the TV Input Select (TS) signal is generated.

Finally, the physical design of the remote control prohibits more than two buttons being pressed simultaneously.

   a) Complete the truth table below for the five output combinational circuit.

P	T	U	C		CU	CD	TS	TP	CP
Power	TV	U/D	CH		CHU	CHD	TV INPUT	TV PWR	CBL PWR
0	0	0	0		0	0	0	0	0
0	0	0	1		1	0	0	0	0
0	0	1	0		1	0	0	0	0
0	0	1	1		0	1	0	0	0
0	1	0	0		0	0	0	0	0
0	1	0	1		0	0	1	0	0
0	1	1	0		0	0	1	0	0
0	1	1	1		X	X	X	X	X
1	0	0	0		0	0	0	1	1
1	0	0	1		0	0	0	1	1
1	0	1	0		0	0	0	1	1
1	0	1	1		X	X	X	X	X
1	1	0	0		0	0	0	1	0
1	1	0	1		X	X	X	X	X
1	1	1	0		X	X	X	X	X
1	1	1	1		X	X	X	X	X

b) Complete the Karnaugh maps below for the Television Input Select (TS) and the Cable Box Power (CP) outputs and determine both a minimum sum of products and a minimum product of sums implementation for each.

UC

PT \	00	01	11	10
00	0	0	0	0
01	0	1	X	1
11	0	X	X	X
10	0	0	X	0

TS = (SOP) $TC + TU$ = (POS) $\overline{P}(U+C)(P+T)$

UC

PT \	00	01	11	10
00	0	0	0	0
01	0	0	X	0
11	0	X	X	X
10	1	1	X	1

CP = (SOP) $P \cdot \overline{T}$ = (POS) $P \cdot \overline{T}$

Problem #5.

The schematic below illustrates a 2 to 1 multiplexer. When the SELECT signal is
a logical 0, IN0 is passed to the OUTPUT; when SELECT is 1, IN1 is passed to
the OUTPUT.
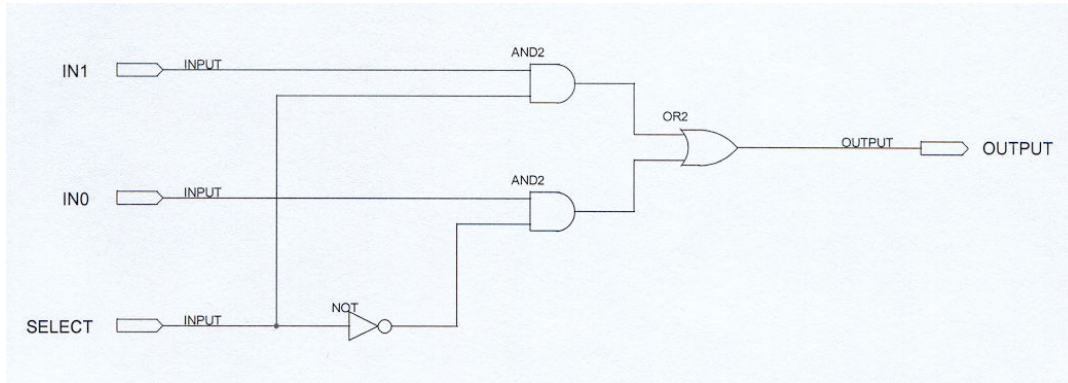
a) Write the structural Verilog code for the 2 to 1 multiplexer using the Verilog
   gates AND, OR and NOT. Include all pertinent declarations and recall that
   the syntax for Verilog gates is f = (out, in1, in2, ...). Your syntax doesn't
   have to be perfect, but all the elements must be included.

```
module mux21 (out,in1,in0,sel);

output out;
input in1,in0,sel;

wire out,in1,in0,sel;
wire a,b,c; //internal nodes

not G1 (a,sel);
and G2 (b,in1,sel);
and G3 (c,in0,a);
or G4 (out,b,c);

endmodule
```

b) A 4 to 1 multiplexer can be constructed from three 2 to 1 multiplexers as shown below. Write the Verilog code to implement a 4 to 1 multiplexer utilizing on the code written in part a) above. Again, the syntax doesn't have to be perfect, but all the elements must be present.
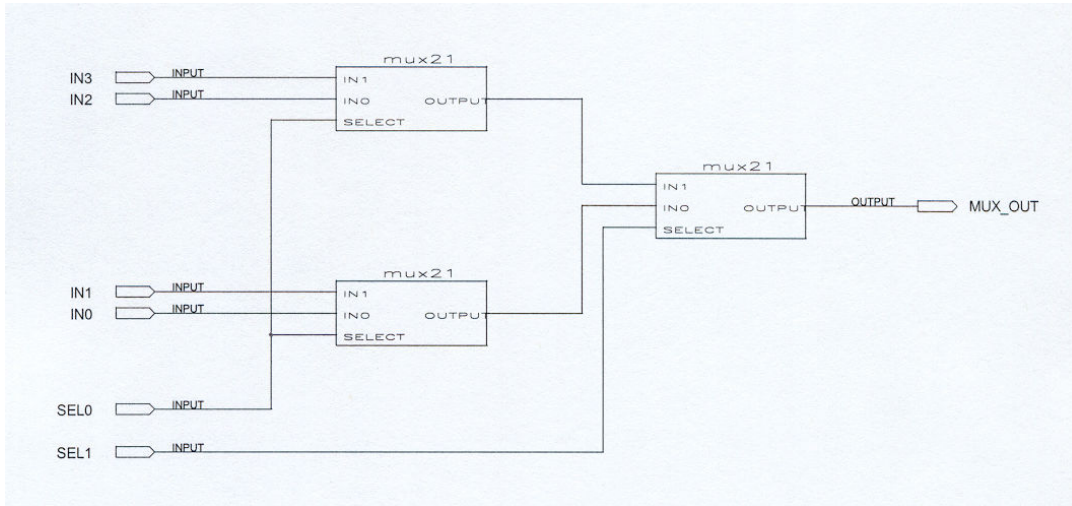

```
module muxverilog(mux_out,in3,in2,in1,in0,sel1,sel0);

output mux_out;
input in3,in2,in1,in0,sel1,sel0;

wire mux_out;
wire in3,in2,in1,in0,sel1,sel0;
wire a,b;

mux21 M1 (a,in3,in2,sel0);
mux21 M2 (b,in1,in0,sel0);
mux21 M3 (mux_out,a,b,sel1);

endmodule
```